Section 7. Reset

HIGHLIGHTS

This section of the manual contains the following topics:

7.1 INTRODUCTION

The Reset module combines all Reset sources and controls the device Master Reset signal, SYSRST. The following is a list of device Reset sources:

- POR: Power-on Reset
- MCLR: Pin Reset
- SWR: RESET Instruction
- WDTR: Watchdog Timer Reset
- BOR: Brown-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Opcode/Uninitialized W Register Reset

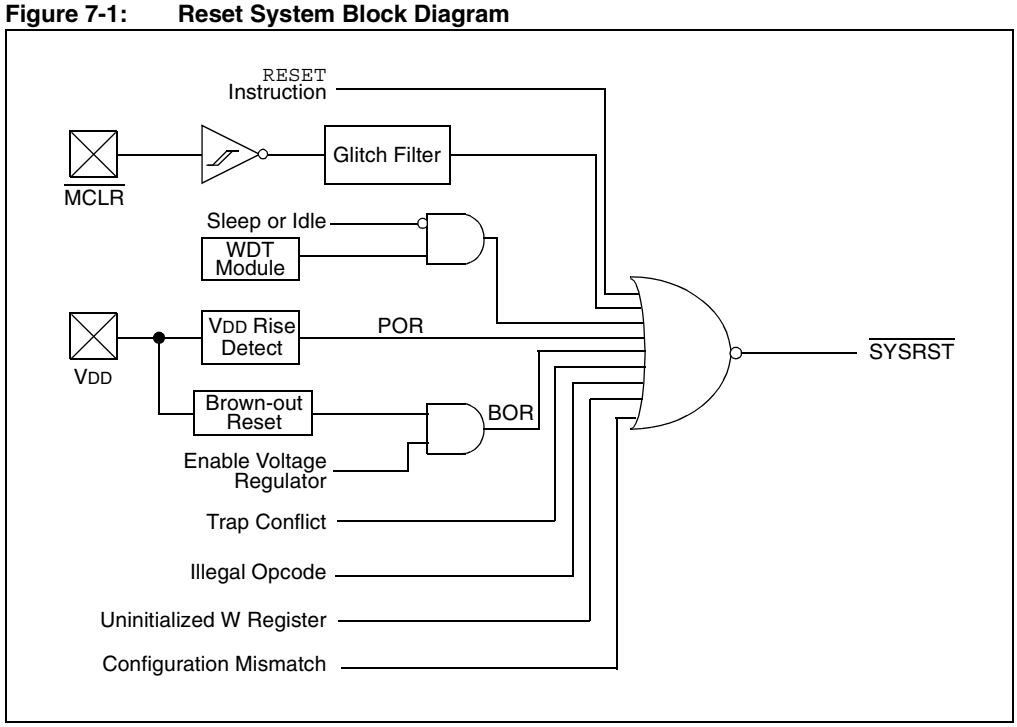
A simplified block diagram of the Reset module is shown in Figure 7-1. Any active source of Reset will make the SYSRST signal active. Many registers associated with the CPU and peripherals are forced to a known "Reset state". Most registers are unaffected by a Reset; their status is unknown on POR and unchanged by all other Resets.

Note:	Refer to the specific peripheral or CPU section of this manual for register Reset states.

All types of device Resets will set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 7-1). A Power-on Reset will clear all bits, except for the BOR and POR bits (RCON<1:0>), which are set. The user may set or clear any of the bits at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software will not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. For more information on the function of these bits, refer to **Section 7.12.1 "Using the RCON Status Bits"**.

Figure 7-1: Reset System Block Diagram



Register 7-1: RCON: Reset Control Register

R/W-0 HS	R/W-0 HS	U-0	U-0	U-0	U-0	R/W-0 HS	R/W-0
TRAPR	IOPUWR	—	—	—	—	CM	VREGS
bit 15							bit 8

R/W-0 HS	R/W-0 HS	R/W-0	R/W-0 HS	R/W-0 HS	R/W-0	R/W-1 HS	R/W-1 HS
EXTR	SWR	SWDTEN(1)	WDTO	SLEEP	IDLE	BOR	POR
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HS = Set in Hardware	HC = Cleared in Hardware
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal Address mode, or uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or uninitialized W Reset has not occurred

bit 13-10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A configuration mismatch Reset has occurred
0 = A configuration mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby Enable bit
1 = Regulator will be active during Sleep
0 = Regulator will go to Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction was executed
0 = A RESET instruction was not executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(1)
1 = WDT is turned on
0 = WDT is turned off

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

bit 3 **SLEEP:** Wake From Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake-up From Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred. Note that BOR is also set after Power-on Reset.
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

Note 1: If the FWDTEN Configuration bit is set (unprogrammed), the WDT is always enabled regardless of the SWDTEN bit setting.

7.2 CLOCK SOURCE SELECTION AT RESET

If clock switching is enabled (OSWEN), the system clock source at device Reset is chosen, as shown in Table 7-1. If clock switching is disabled, the system clock source is always selected according to the oscillator Configuration bits. Refer to **Section 6. "Oscillator"** for further details.

Table 7-1: Oscillator Selection vs. Type of Reset (Clock Switching Enabled)

Reset Type	Clock Source Selected Based On
POR	Oscillator Configuration Bits (FNOSC2:FNOSC0)
BOR	
CM	
$\overline{\text{MCLR}}$	COSC Control bits (OSCCON<14:12>)
WDTR	
SWR	
TRAPR	
IOPUWR	

7.3 POWER-ON RESET (POR)

The POR monitors the core power supply for adequate voltage levels to ensure proper chip operation. There are two threshold voltages associated with a Power-on Reset (POR). The first voltage is the device threshold voltage, VPOR. The device threshold voltage is the voltage at which the POR module becomes operable. The second voltage associated with a POR event is the POR circuit threshold voltage. Once the correct threshold voltage is detected, a power-on event occurs and the POR module hibernates to minimize current consumption.

A power-on event generates an internal Power-on Reset pulse when a VDD rise is detected. The device supply voltage characteristics must meet the specified starting voltage and rise rate requirements to generate the POR pulse. In particular, VDD must fall below VPOR before a new POR is initiated. For more information on the VPOR and VDD rise rate specifications, refer to the **"Electrical Characteristics"** section of the specific device data sheet

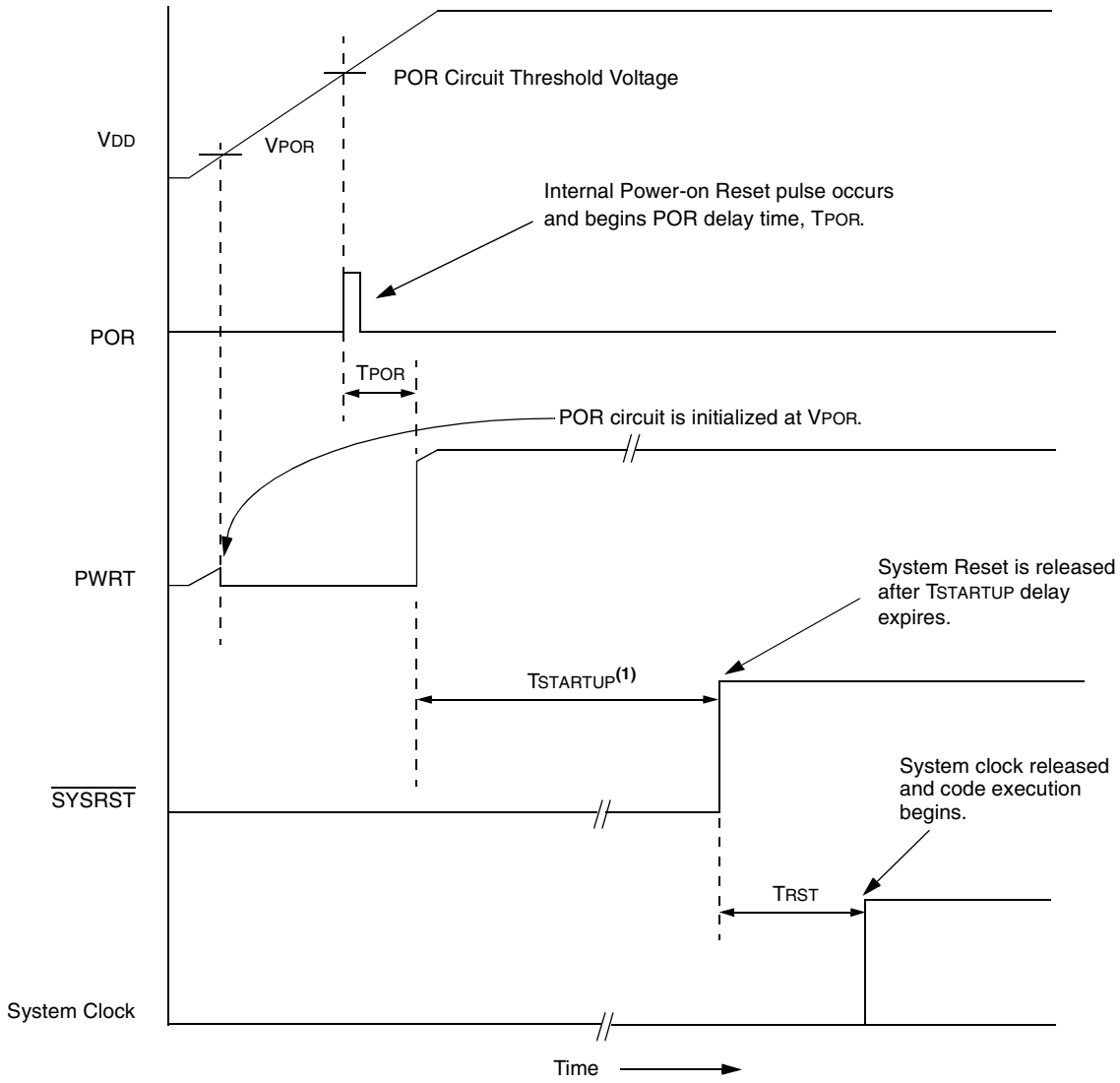
The POR pulse resets the POR timer and places the device in the Reset state. The POR also selects the device clock source identified by the oscillator Configuration bits.

After the Power-on Reset pulse is generated, the POR circuit inserts a small delay, TPOR, which is nominally 10 μs and ensures that internal device bias circuits are stable. After the expiration of TPOR, a delay, TSTARTUP, is always inserted. The TSTARTUP parameter depends on whether the on-chip voltage regulator is enabled or disabled. When the on-chip voltage regulator is enabled, it takes approximately 10 μs for it to generate proper voltage level. During this time, code execution is disabled. TSTARTUP is applied every time the device resumes operation after any power-down. If the regulator is disabled, a separate Power-up Timer (PWRT) is automatically enabled. The PWRT adds a fixed 64 ms nominal delay at device start-up. The Power-up Timer is used to extend the duration of a power-up sequence when the on-chip voltage regulator is disabled and the core is supplied from an external power supply. Hence, the TSTARTUP delay can either be the on-chip voltage regulator output delay, designated as TVREG, or the power-up timer delay, designated as TPWRT. The power-on event will set the BOR and POR status bits (RCON<1:0>).

Code execution is delayed further by a small delay, designated as TRST. The TRST delay is required to transfer the configuration values from Flash Configuration Words in the program memory into the Configuration registers, and occurs after any device Reset. $\overline{\text{SYSRST}}$ is released and the device is no longer held in Reset, but the device clocks are prevented from running during TRST, as shown in Figure 7-2. Once all of the delays have expired, the system clock is released and code execution can begin.

Refer to **Section 7.15 "Electrical Specifications"** for more information on the values of the delay parameters.

Figure 7-2: POR Module Timing Sequence for Rising VDD



Note 1: TSTARTUP = TVREG if on-chip regulator is enabled, or TPWRT if on-chip regulator is disabled.

Note:	When the device exits the Reset condition (begins normal operation), the device operating parameters (voltage, frequency, temperature, etc.) must be within their operating ranges; otherwise, the device will not function correctly. The user must ensure that the delay between the time power is first applied and the time $\overline{\text{SYSRST}}$ becomes inactive is long enough to get all operating parameters within specification.

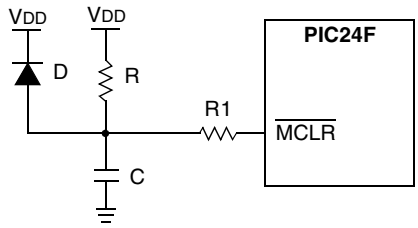
7.3.1 Using the POR Circuit

To take advantage of the POR circuit, just tie the $\overline{MCLR}$ pin directly to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise time for VDD is required. Refer to the **"Electrical Characteristics"** section of the specific device data sheet for more information.

Depending on the application, a resistor may be required between the $\overline{MCLR}$ pin and VDD. This resistor can be used to decouple the $\overline{MCLR}$ pin from a noisy power supply rail.

Figure 7-3 shows a possible POR circuit for a slow power supply ramp up. The external Power-on Reset circuit is only required if the device would exit Reset before the device VDD is in the valid operating range. The diode, D, helps discharge the capacitor quickly when VDD powers down.

Figure 7-3: External Power-on Reset Circuit (For Slow VDD Rise Time)



Note 1: The value of R should be low enough so that the voltage drop across it does not violate the VIH specification of the $\overline{MCLR}$ pin.

2: R1 will limit any current flowing into $\overline{MCLR}$ from external capacitor C in the event of $\overline{MCLR}$/VPP pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

7.4 $\overline{MCLR}$ RESET

Whenever the $\overline{MCLR}$ pin is driven low, the device asynchronously asserts $\overline{SYSRST}$, provided the input pulse on $\overline{MCLR}$ is longer than a certain minimum width, SY10 (see **Section 7.15 "Electrical Specifications"**). When the $\overline{MCLR}$ pin is released, $\overline{SYSRST}$ is also released. The Reset vector fetch starts after the expiration of the TRST delay, starting from the $\overline{SYSRST}$ release. The processor continues to use the existing clock source that was in use before the $\overline{MCLR}$ Reset occurred. The EXTR status bit (RCON<7>) is set to indicate the $\overline{MCLR}$ Reset.

7.5 SOFTWARE RESET INSTRUCTION (SWR)

Whenever the RESET instruction is executed, the device asserts $\overline{SYSRST}$. This Reset state does not re-initialize the clock. The clock source in effect prior to the RESET instruction remains. $\overline{SYSRST}$ is released at the next instruction cycle, but the Reset vector fetch starts only after the TRST delay.

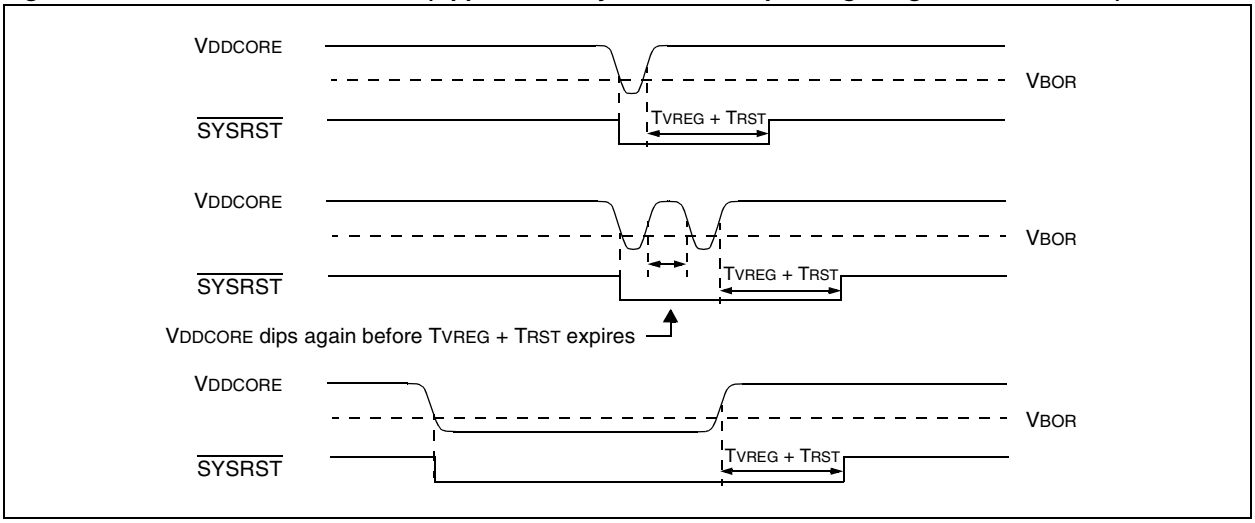
7.6 WATCHDOG TIME-OUT RESET (WDTR)

Whenever a Watchdog time-out occurs, the device asynchronously asserts $\overline{SYSRST}$. The clock source remains unchanged. Note that a WDT time-out during Sleep or Idle mode will wake-up the processor, but NOT reset the processor. For more information, refer to **Section 9. "Watchdog Timer (WDT)"**.

7.7 BROWN-OUT RESET (BOR)

When the on-chip regulator is enabled, PIC24F family devices have a simple brown-out capability. BOR is applicable only when the regulator is enabled. If the voltage supplied to the regulator is inadequate to maintain a regulated level, the regulator Reset circuitry will generate a Brown-out Reset. This event is captured by the BOR flag bit (RCON<0>). Refer to **Section 7.15 "Electrical Specifications"** for further details.

Figure 7-4: Brown-out Situations (Applicable only when On-Chip Voltage Regulator is Enabled)



7.8 CONFIGURATION MISMATCH RESET

To maintain the integrity of the stored configuration values, all device Configuration bits are implemented as a complementary set of register bits. For each bit, as the actual value of the register is written as '1', a complementary value, '0', is stored into its corresponding background register and vice versa. The bit pairs are compared every time, including Sleep mode. During this comparison, if the Configuration bit values are not found opposite to each other, a configuration mismatch event is generated which causes a device Reset.

If a device Reset occurs as a result of a configuration mismatch, the CM status bit (RCON<9>) is set.

7.9 TRAP CONFLICT RESET

A Trap Conflict Reset occurs when a hard trap and a soft trap occur at the same time. The TRAPR status bit (RCON<15>) is set on this event. Refer to **Section 8. "Interrupts"** for more information on traps.

7.10 ILLEGAL OPCODE RESET

A device Reset is generated if the device attempts to execute an illegal opcode value that was fetched from program memory. If a device Reset occurs as a result of an illegal opcode value, the IOPUWR status bit (RCON<14>) is set.

The Illegal Opcode Reset function can prevent the device from executing program memory sections that are used to store constant data. To take advantage of the Illegal Opcode Reset, use only the lower 16 bits of each program memory section to store the data values. The upper 8 bits should be programmed with 3Fh, which is an illegal opcode value.

7.11 UNINITIALIZED W REGISTER RESET

The W register array (with the exception of W15) is cleared during all Resets and is considered uninitialized until written to. An attempt to use an uninitialized register as an Address Pointer causes a device Reset and sets the IOPUWR status bit (RCON<14>).

7.12 REGISTERS AND STATUS BIT VALUES

Status bits from the RCON register are set or cleared differently in different Reset situations, as indicated in Table 7-2.

Table 7-2: Status Bits, Their Significance and the Initialization Condition for RCON Register

Condition	Program Counter	TRAPR	IOPUWR	EXTR	SWR	WDTO	SLEEP	IDLE	CM	BOR	POR	STKEPR
Power-on Reset	000000h	0	1	1	1	0	0	0	u	1	1	0
RESET Instruction	000000h	0	0	0	1	0	0	0	u	0	0	0
Brown-out Reset	000000h	0	0	0	0	0	0	0	u	0	0	0
$\overline{\text{MCLR}}$ during Run Mode	000000h	0	0	1	0	0	0	0	u	0	0	0
$\overline{\text{MCLR}}$ during Idle Mode	000000h	0	0	1	0	0	0	1	u	0	0	0
$\overline{\text{MCLR}}$ during Sleep Mode	000000h	0	0	1	0	0	1	0	u	0	0	0
WDT Time-out Reset during Run Mode	000000h	0	0	0	0	1	0	0	u	0	0	0
WDT Time-out Reset during Idle Mode	PC + 2	0	0	0	0	1	0	0	u	0	0	0
WDT Time-out Reset during Sleep Mode	PC + 2	0	0	0	0	1	1	1	u	0	0	0
Stack Overflow Reset	000000h	0	0	0	0	0	0	0	u	0	0	1
Stack Underflow Reset	000000h	0	0	0	0	0	0	0	u	0	0	1
Trap Event Reset	000000h	1	0	0	0	0	0	0	u	0	0	0
Illegal Opcode/ Uninitialized WREG	000000h	0	1	0	0	0	0	0	u	0	0	0
Configuration Word Mismatch Reset	000000h	u	u	u	u	u	u	u	1	u	u	u
Interrupt Exit from Idle Mode	PC + 2(1)	0	0	0	0	0	0	1	u	0	0	0
Interrupt Exit from Sleep Mode	PC + 2(1)	0	0	0	0	0	1	0	u	0	0	0
Idle Mode (execute PWRSAV 1)	PC + 2	0	0	0	0	0	0	1	u	0	0	0
Sleep Mode (execute PWRSAV 0)	PC + 2	0	0	0	0	0	1	0	u	0	0	0

Legend: u = unchanged

Note 1: Program counter is loaded with PC + 2 if the interrupt priority is less than, or equal to, the CPU interrupt priority level. Program counter is loaded with the hardware vector address if the interrupt priority is greater than the CPU interrupt priority level.

7.12.1 Using the RCON Status Bits

The user can read the RCON register after any device Reset to determine the cause of the Reset. Table 7-3 provides a summary of the Reset flag bit operation.

Note:	The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset will be meaningful.

Table 7-3: Reset Flag Bit Operation

Flag Bit	Set by:	Cleared by:
TRAPR (RCON<15>)	Trap conflict event	POR
IOPWR (RCON<14>)	Illegal opcode or uninitialized W register access	POR
EXTR (RCON<7>)	$\overline{\text{MCLR}}$ Reset	POR
SWR (RCON<6>)	RESET instruction	POR
WDTO (RCON<4>)	WDT time-out	PWRSAV instruction, POR
SLEEP (RCON<3>)	PWRSAV #SLEEP instruction	POR, CLRWDT instruction
IDLE (RCON<2>)	PWRSAV #IDLE instruction	POR, CLRWDT instruction
BOR (RCON<1>)	POR, BOR	—
POR (RCON<0>)	POR	—

Note: All Reset flag bits may be set or cleared by the user software.

7.13 DEVICE RESET TO CODE EXECUTION START TIME

The delay between the end of a Reset event and when the device actually begins to execute code is determined by two main factors: the type of Reset, and the system clock source coming out of the Reset. The code execution start time for various types of device Resets are summarized in Table 7-4. Individual delays are characterized in **Section 7.15 "Electrical Specifications"**.

Table 7-4: Code Execution Start Time for Various Device Resets

Reset Type	Clock Source	Code Execution Delay	System Clock Delay	FSCM Delay	Notes
POR	EC, FRC, FRCDIV, LPRC	TPOR + TSTARTUP + TRST	—	—	**1, 2, 3**
	ECPLL, FRCPLL	TPOR + TSTARTUP + TRST	TLOCK	TFSCM	**1, 2, 3, 5, 6**
	XT, HS, SOSC	TPOR + TSTARTUP + TRST	TOST	TFSCM	**1, 2, 3, 4, 6**
	XTPLL	TPOR + TSTARTUP + TRST	TOST + TLOCK	TFSCM	**1, 2, 3, 4, 5, 6**
BOR	EC, FRC, FRCDIV, LPRC	TSTARTUP + TRST	—	—	**2, 3**
	ECPLL, FRCPLL	TSTARTUP + TRST	TLOCK	TFSCM	**2, 3, 5, 6**
	XT, HS, SOSC	TSTARTUP + TRST	TOST	TFSCM	**2, 3, 4, 6**
	XTPLL	TSTARTUP + TRST	TOST + TLOCK	TFSCM	**2, 3, 4, 5, 6**
$\overline{\text{MCLR}}$	Any Clock	TRST	—	—	**3**
WDT	Any Clock	TRST	—	—	**3**
Software	Any clock	TRST	—	—	**3**
Illegal Opcode	Any Clock	TRST	—	—	**3**
Uninitialized W	Any Clock	TRST	—	—	**3**
Trap Conflict	Any Clock	TRST	—	—	**3**

Note 1: TPOR = Power-on Reset delay.

2: TSTARTUP = TVREG if on-chip regulator is enabled, or TPWRT if on-chip regulator is disabled.

3: TRST = Internal state Reset time (20 μs nominal).

4: TOST = Oscillator Start-up Timer.

5: TLOCK = PLL lock time.

6: TFSCM = Fail-Safe Clock Monitor delay.

For Power-on Reset, the system Reset signal, $\overline{\text{SYSRST}}$, is released after the POR delay time (TPOR) and the TSTARTUP delay time expire. For Brown-out Reset, $\overline{\text{SYSRST}}$ is released after the TSTARTUP delay time expires. For all other Resets, the system Reset signal, $\overline{\text{SYSRST}}$, is released immediately after the Reset condition is removed. For all Resets, the TRST delay starts after the $\overline{\text{SYSRST}}$ is released; code execution starts after the expiration of TRST.

The time that the device actually begins to execute code also depends on the system oscillator delays, which include the Oscillator Start-up Timer delay (TOST) and the PLL lock time (TLOCK). The OST and PLL lock times run parallel to the applicable code execution delay times.

7.13.1 POR and Long Oscillator Start-up Times

The oscillator start-up circuitry and its associated delay timers are not linked to the device Reset delays that occur at power-up. Some crystal circuits (especially low frequency crystals) will have a relatively long start-up time. Therefore, one or more of the following conditions is possible after $\overline{\text{SYSRST}}$ is released:

- The oscillator circuit has not begun to oscillate.
- The oscillator start-up timer has NOT expired (if a crystal oscillator is used).
- The PLL has not achieved a lock (if PLL is used).

The device will not begin to execute code until a valid clock source has been released to the system. Therefore, the oscillator and PLL start-up delays must be considered when the Reset delay time must be known.

7.13.2 Fail-Safe Clock Monitor (FSCM) and Device Resets

The Fail-Safe Clock Monitor (FSCM) is designed to allow the device to continue to operate even in the event of an oscillator failure. The FSCM function is enabled by clearing the FCKSM<1:0> bits in the FOSC (Oscillator Configuration) register. FSCM will operate, if enabled, during operational modes and the Idle mode. It does not operate during Sleep mode.

If the FSCM function is enabled, the LPRC internal oscillator will run at all times (except during Sleep) and will not be subject to control by the SWDTEN bit. Because the LPRC oscillator will be running at all times, this will cause a slight increase in power consumption.

The FSCM clock will be 4 kHz and generated by dividing the LPRC clock by 128. The FSCM clock monitors the system clock during the rising edge. If the system clock is not present for one complete cycle of FSCM, the clock failure trap will be set; thus, the detection time for a clock failure is approximately 250 μS.

In the event of an oscillator failure with FSCM enabled, the FSCM will generate a clock fail trap and will switch the system clock over to the FRC oscillator. If the device is in Idle mode, the clock fail trap will cause a wake-up and return to operational mode. The user will then have the option to either attempt to restart the oscillator or execute a controlled shutdown.

7.13.2.1 FSCM DELAY FOR CRYSTAL AND PLL CLOCK SOURCES

When the system clock source is provided by a crystal oscillator and/or the PLL, a small delay, TFSCM, will automatically be inserted after the POR and PWRT delay times. The FSCM will not begin to monitor the system clock source until this delay expires. The FSCM delay time is nominally 100 μs and provides additional time for the oscillator and/or PLL to stabilize.

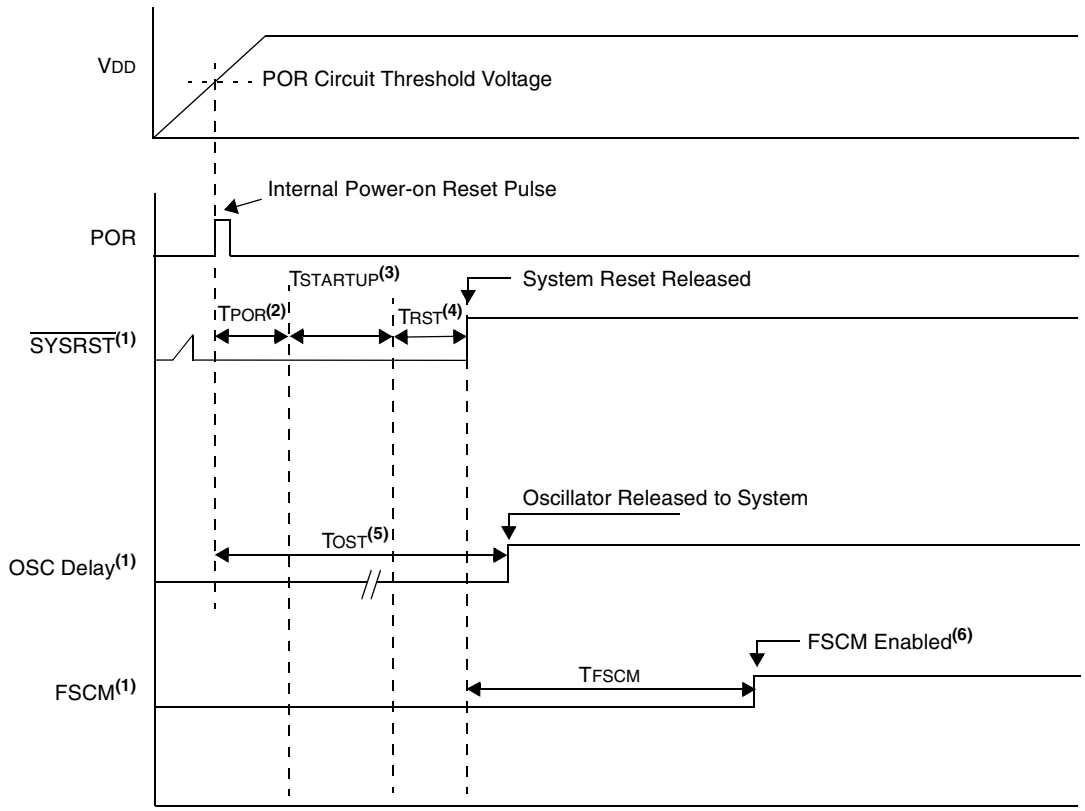
7.13.3 Examples of Device Start-up Time Lines

Figure 7-5 through Figure 7-8 show graphical time lines of the delays associated with device Reset for several operating scenarios. The individual delays are characterized in **Section 7.15 "Electrical Specifications"**.

Figure 7-5 shows the delay time line when a crystal oscillator is used as the system clock. The internal Power-on Reset pulse occurs at the VPOR threshold. TPOR, TSTARTUP and TRST delays occur after the internal Power-on Reset pulse.

The FSCM, if enabled, begins to monitor the system clock for activity when the FSCM delay expires. Figure 7-5 shows that the oscillator start-up delay (TOST) expires before the Fail-Safe Clock Monitor (FSCM) is enabled. However, it is possible that this delay may not expire until after FSCM is enabled. If a valid clock source is not available at this time, the device will automatically switch to the FRC oscillator and a clock failure trap will be generated. The user can switch to the desired crystal oscillator in the Trap Service Routine.

Figure 7-5: Device Reset Delay, Crystal (XT/HS/SOSC) Clock Source



Note 1: Delay times shown are not drawn to scale.

2: TPOR = Power-on Reset delay.

3: TSTARTUP = TVREG if on-chip regulator enabled or TPWRT if on-chip regulator disabled.

4: TRST = Internal state Reset time.

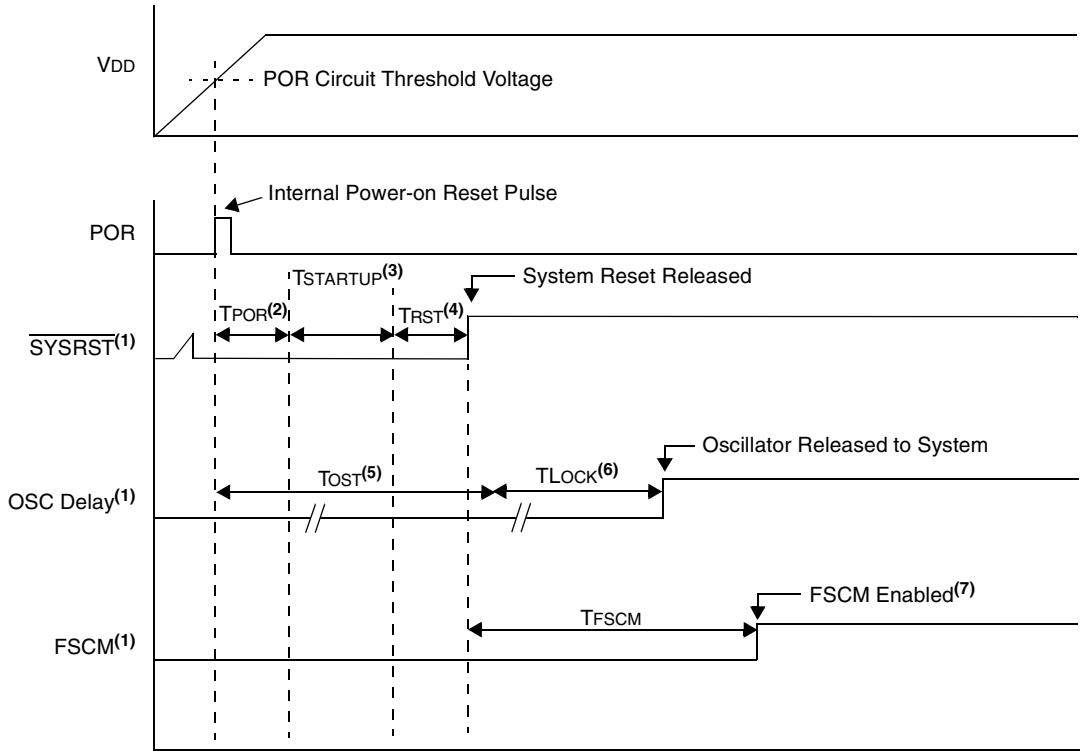
5: TOST = Oscillator Start-up Timer. A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.

6: FSCM, if enabled, monitors system clock at expiration of TPOR + TSTARTUP + TRST +TFSCM.

The Reset time line shown in Figure 7-6 is similar to that shown in Figure 7-5, except that the PLL has been enabled, which increases the oscillator stabilization time.

The FSCM, if enabled, will begin to monitor the system clock after TFSCM expires. Figure 7-6 shows that the oscillator and PLL delays expire before the Fail-Safe Clock Monitor (FSCM) is enabled. However, it is possible that these delays may not expire until after FSCM is enabled. If a valid clock source is not available at this time, the device will automatically switch to the FRC oscillator and a clock failure trap will be generated. The user can switch to the desired crystal oscillator in the Trap Service Routine.

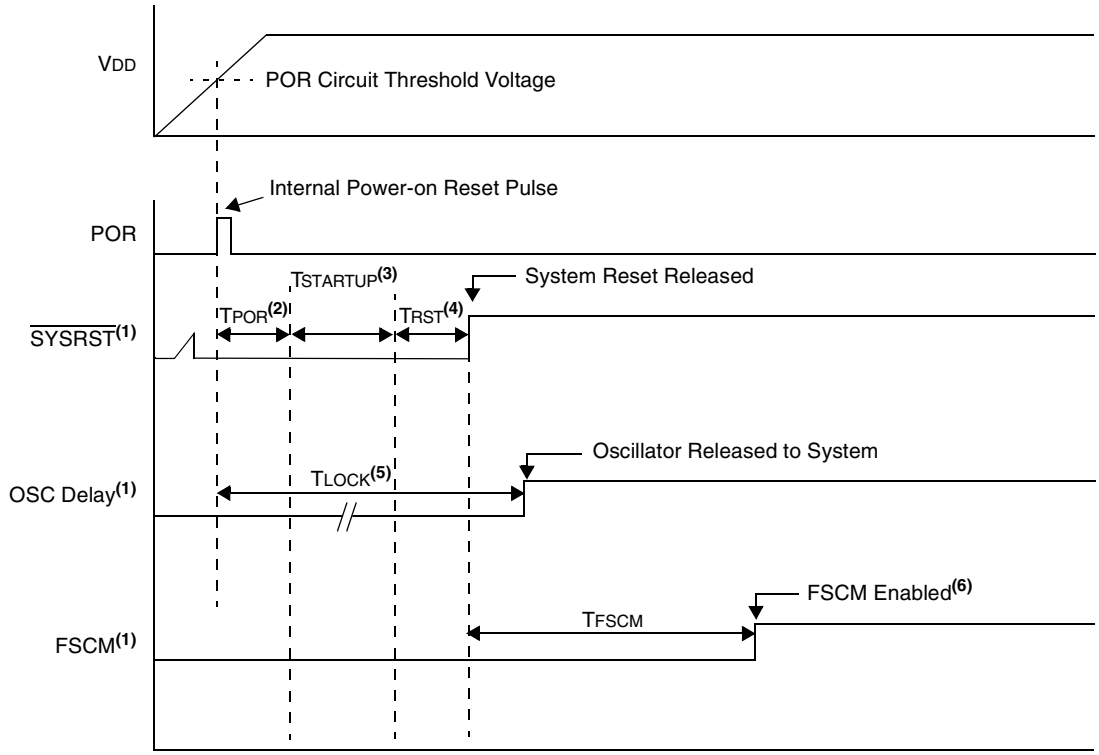
Figure 7-6: Device Reset Delay, Crystal (XT/HS/SOSC) + PLL Clock Source



Note 1: Delay times shown are not drawn to scale.
2: TPOR = Power-on Reset delay.
3: TSTARTUP = TVREG if on-chip regulator enabled or TPWRT if on-chip regulator disabled.
4: TRST = Internal state Reset time.
5: TOST = Oscillator Start-up Timer. A 10-bit counter counts 1024 oscillator periods before releasing the oscillator clock to the system.
6: TLOCK not inserted when PLL is disabled.
7: FSCM, if enabled, monitors system clock at expiration of TPOR + TSTARTUP + TRST +TFSCM.

The Reset time line in Figure 7-7 shows an example when the ECPLL clock source is used as the system clock. This example is similar to the one shown in Figure 7-6, except that the Oscillator Start-up Timer delay, TOST, does not occur.

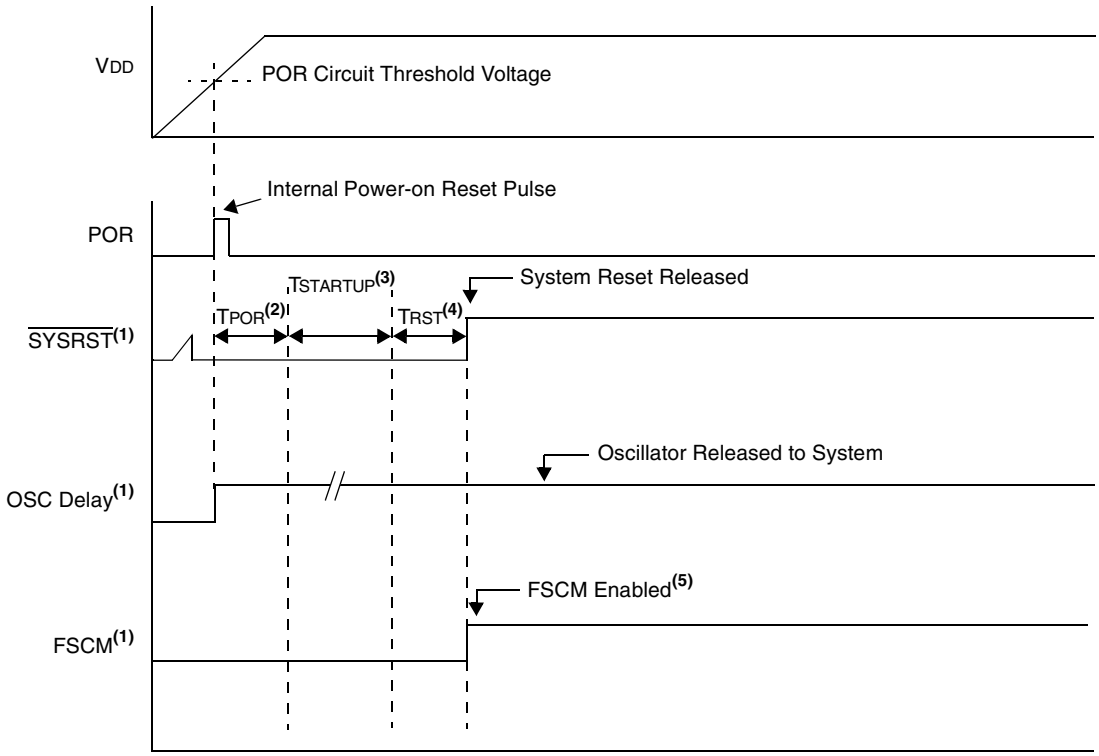
Figure 7-7: Device Reset Delay, ECPLL Clock(7)



Note 1: Delay times shown are not drawn to scale.
2: TPOR = Power-on Reset delay.
3: TSTARTUP = TVREG if on-chip regulator enabled or TPWRT if on-chip regulator disabled.
4: TRST = Internal state Reset time.
5: TLOCK not inserted when PLL is disabled.
6: FSCM, if enabled, monitors system clock at expiration of TPOR + TSTARTUP + TRST +TFSCM.
7: Refer to **Section 7.15 "Electrical Specifications"** for typical values of the delays.

The Reset time line shown in Figure 7-8 shows an example where an EC without PLL, or FRC system clock source is selected.

Figure 7-8: Device Reset Delay, EC or FRC Clock(6)



Note 1: Delay times shown are not drawn to scale.
2: TPOR = Power-on Reset delay.
3: TSTARTUP = TVREG if on-chip regulator enabled or TPWRT if on-chip regulator disabled.
4: TRST = Internal state Reset time.
5: FSCM, if enabled, monitors system clock at expiration of TPOR + TSTARTUP + TRST +TFSCM.
6: Refer to **Section 7.15 "Electrical Specifications"** for typical values of the delays.

7.14 SPECIAL FUNCTION REGISTER RESET STATES

Most of the special function registers (SFRs) associated with the PIC24F CPU and peripherals are reset to a particular value at a device Reset. The SFRs are grouped by their peripheral or CPU function and their Reset values are specified in the corresponding section of this manual.

The Reset value for each SFR does not depend on the type of Reset, with the exception of two registers. The Reset value for the Reset Control register, RCON, will depend on the type of device Reset. The Reset value for the Oscillator Control register, OSCCON, will depend on the type of Reset and the programmed values of the oscillator Configuration bits in the FOSC Device Configuration register (see Table 7-1).

7.15 ELECTRICAL SPECIFICATIONS

Figure 7-9: Brown-out Reset Characteristics

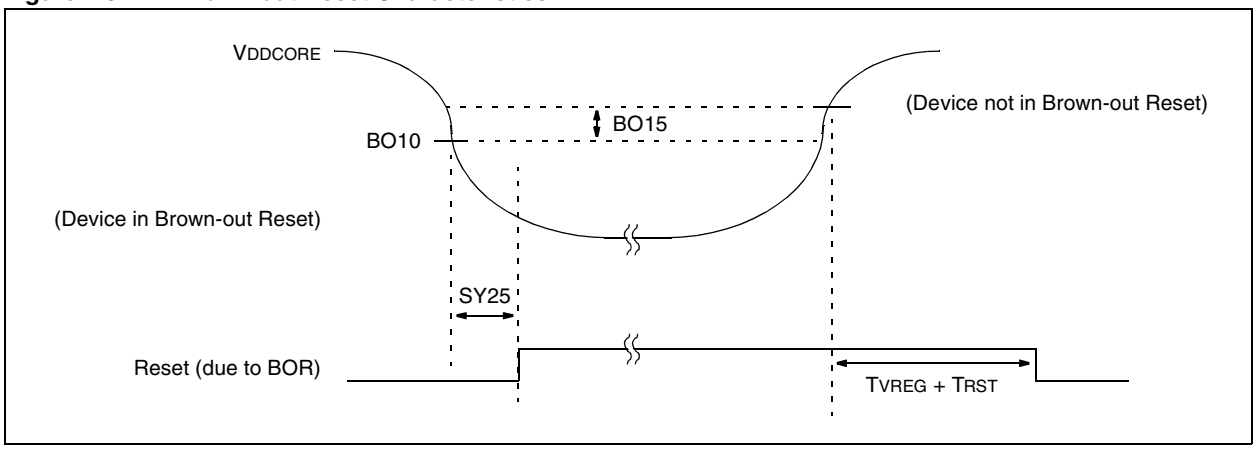


Figure 7-10: Reset, Watchdog Timer, Oscillator Start-up Timer and Power-up Timer Timing Characteristics

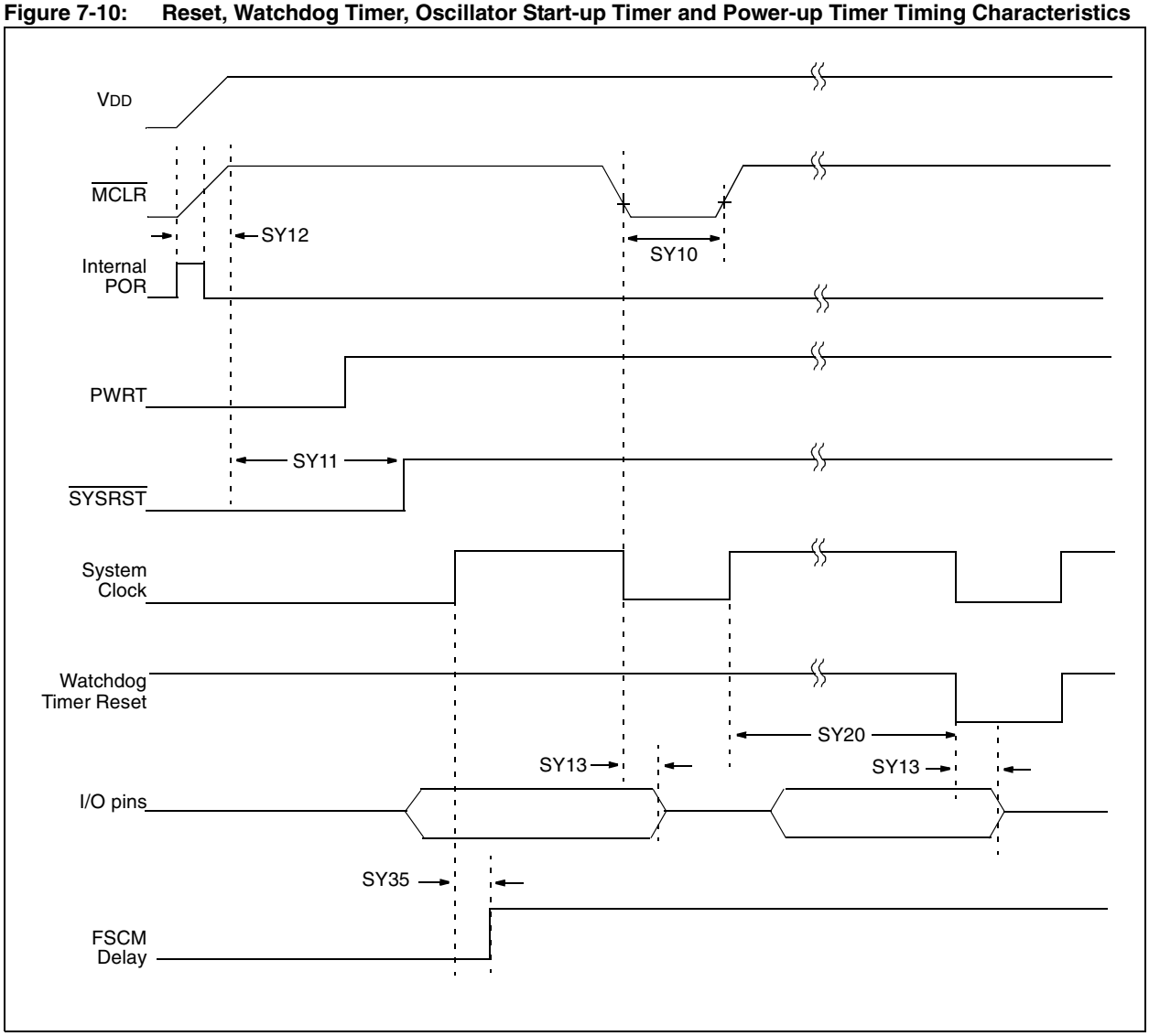


Table 7-5: Electrical Characteristics: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
BO10	VBOR	BOR Voltage on VDD Transition, High-to-Low	2.3	—	2.7	V	Voltage regulator enabled
BO15	VBHYS	BOR Hysteresis	—	5	—	mV	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

Table 7-6: Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer and Brown-out Reset Timing Requirements

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
SY10	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	µs	
SY11	TPWRT	Power-up Timer Period	50	64	90	ms	Voltage regulator enabled
SY12	TPOR	Power-on Reset Delay	1	5	10	µs	
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	—	100	ns	
SY20	TWDT	Watchdog Timer Time-out Period	0.85	1.0	1.15	ms	1:32 prescaler
			3.4	4.0	4.6	ms	1:128 prescaler
SY25	TBOR	Brown-out Reset Pulse Width	1	—	—	µs	VDD ≤ VBOR, voltage regulator disabled
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	2	2.3	µs	
	TRST	Configuration Update Time	—	7.8	9.8	µs	
	TVREG	On-Chip Voltage Regulator Output Delay	—	10	—	µs	

Note 1: Data in "Typ" column is at 3.3V, 25°C unless otherwise stated.

7.16 DESIGN TIPS

Question 1: ***How do I use the RCON register?***

Answer: The initialization code after a Reset should examine RCON and confirm the source of the Reset. In certain applications, this information can be used to take appropriate action to correct the problem that caused the Reset to occur. All Reset status bits in the RCON register should be cleared after reading them to ensure the RCON value will provide meaningful results after the next device Reset.

Question 2: ***The BOR module does not have the programmable trip points that my application needs. How can I work around this?***

Answer: The BOR circuitry is used to avoid the violation of V/f specification of the device. In many devices, the minimum voltage for the full speed operation is much higher. Therefore, a programmable BOR circuit is needed to provide the multiple speed option. The PIC24F devices support full speed operation at a much lower voltage and the simple BOR module is enough. If the device operating voltage drops to a value where full speed operation isn't possible, then BOR is asserted. If the device is in a non-BOR state, then full speed operation is valid.

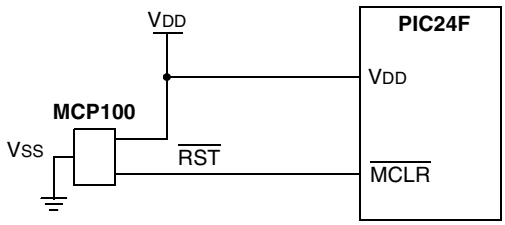
Question 3: ***I initialized a W register with a 16-bit address; why does the device appear to reset when I attempt to use the register as an address?***

Answer: Because all data addresses are 16-bit values, the uninitialized W register logic only recognizes that a register has been initialized correctly if it was subjected to a word load. Two byte moves to a W register, even if successive, will not work, resulting in a device Reset if the W register is used as an Address Pointer in an operation.

Question 4: ***I am disabling the on-board voltage regulator. What should I do to achieve BOR protection?***

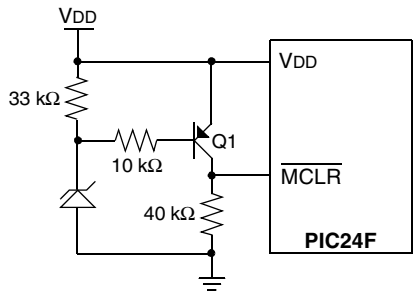
Answer: The following figures show the possible circuitry for external brown-out protection.

Figure 7-11: External Brown-out Protection Using the MCP100



This circuit will activate Reset when VDD goes below (VZ + 0.7V), where VZ = Zener voltage.

Figure 7-12: Brown-out Reset Circuit



Note: Resistors should be adjusted for the characteristics of the transistor.

7.17 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the PIC24F device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to Reset are:

Title	Application Note #
Power-up Trouble Shooting	AN607
Power-up Considerations	AN522

Note: Please visit the Microchip web site (www.microchip.com) for additional application notes and code examples for the PIC24F family of devices.

7.18 REVISION HISTORY

Revision A (September 2006)

This is the initial released revision of this document.

NOTES: